

**Digital Logic Lab Assignment 13 & 14**

* To construct a full subtractor using required decoders
* To construct a full adder using required decoders
* To verify the operation of 2 X 4 encoder
* To verify the operation of 4 X 2 encoder
* To verify the operation of 8 X 3 encoder
* To verify the operation of 16 X 4 encoder

**Submitted By**

Gaurav Chaulagain

Year I / SEM I

017BSCIT01

**Submitted To**

Signature Remarks

Er. Rajan Karmacharya

Lecturer, Dept. of Computer Science

Er. Saugat Sigdel

Lecturer, Dept. of Computer Science

**OBJECTIVE 1.1**

**To Construct a full subtractor using a decoder**

**THEORY:**

A decoder is a combinational circuit that converts binary information from n-input lines to a maximum number of 2n unique output lines. The basic function of decoder is to detect the presence of a specified combination of bits on its inputs and to indicate the presence of that code by a specified output level. It gives only one high output at a time.

A full subtractor can be constructed by using a BCD decoder and 2 AND gates.

**Boolean Expression:**

D=∑(1,2,4,7)

B=∑(1,2,3,7)

**Block Diagram:**

A

B

C

Difference

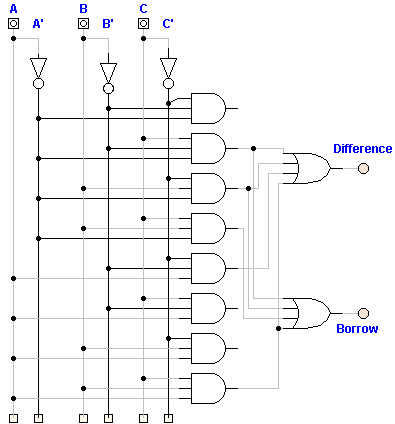
AND gate

**3 x 8 Decoder**

AND gate

Borrow

**Fig. Block diagram of a full subtractor using a decoder**

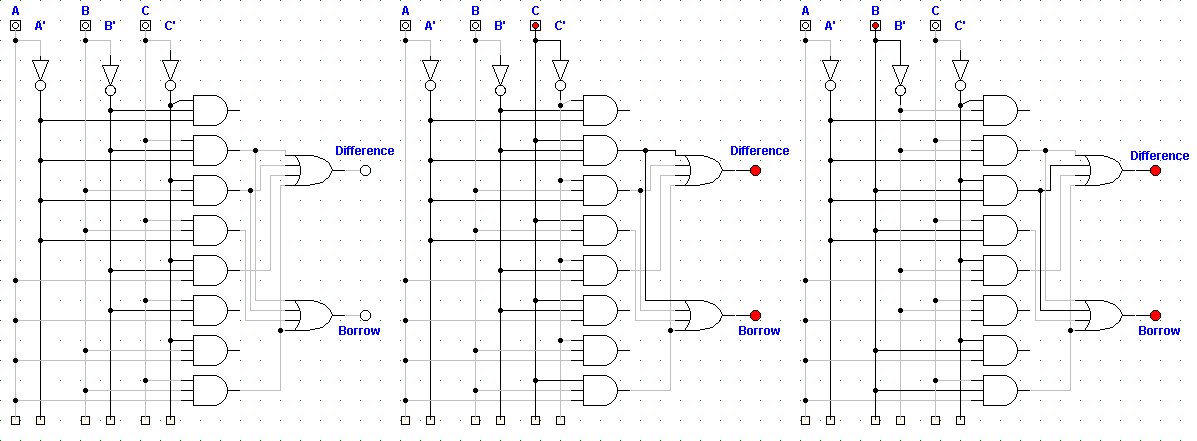
**Circuit Diagram:**

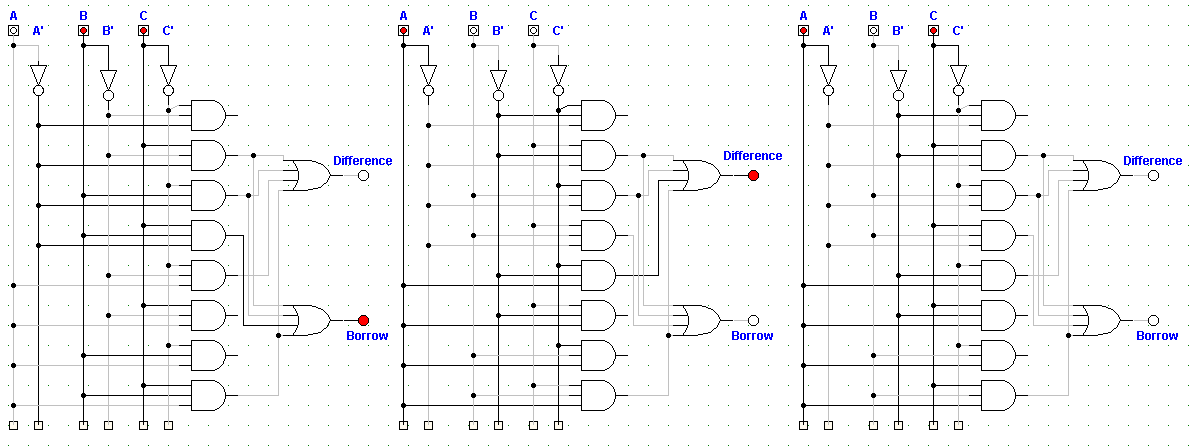
**Fig. Circuit diagram of a full subtractor using a decoder**

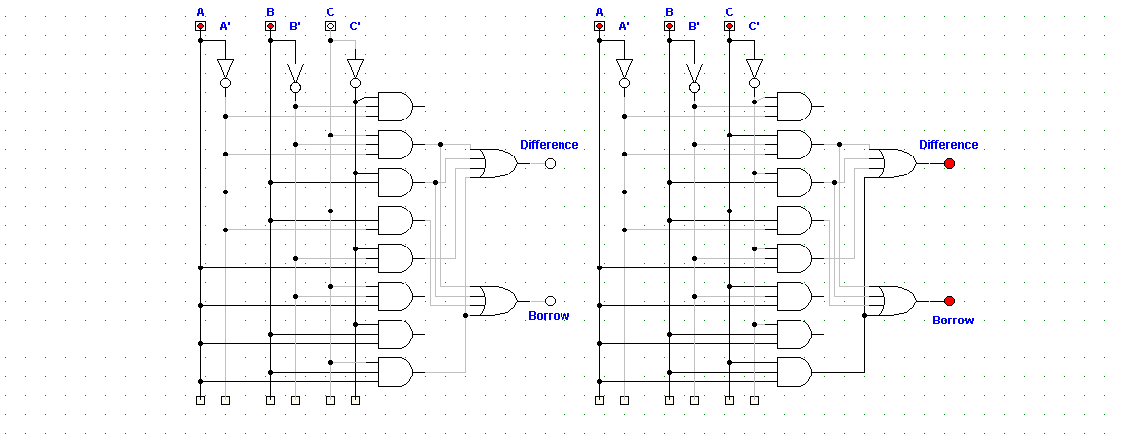
**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | |
| **A** | **B** | **C** | **Bo** | **D** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Observation:**







**Observation Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | |
| **A** | **B** | **C** | **Bo** | **D** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Conclusion:**

Thus, the operation of full subtractor using decoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/3036

http://answers.yahoo.com/question/index?qid=20090215044042AAxpa1T

**OBJECTIVE 1.2**

**To Construct a full adder using a decoder**

**THEORY:**

A decoder is a combinational circuit that converts binary information from n-input lines to a maximum number of 2n unique output lines. The basic function of decoder is to detect the presence of a specified combination of bits on its inputs and to indicate the presence of that code by a specified output level. It gives only one high output at a time.

A full adder can be constructed by using a BCD decoder and 2 AND gates.

**Boolean Expression:**

Carry=∑(3,5,6,7)

Sum =∑(1,2,4,7)

**Block Diagram:**

A

B

C

Sum

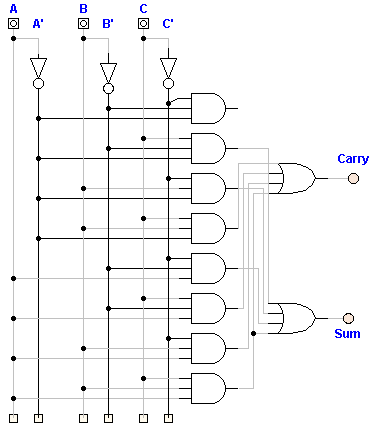
AND gate

**3 x 8 Decoder**

Carry

AND gate

**Fig. Circuit diagram of a full adder using a decoder**

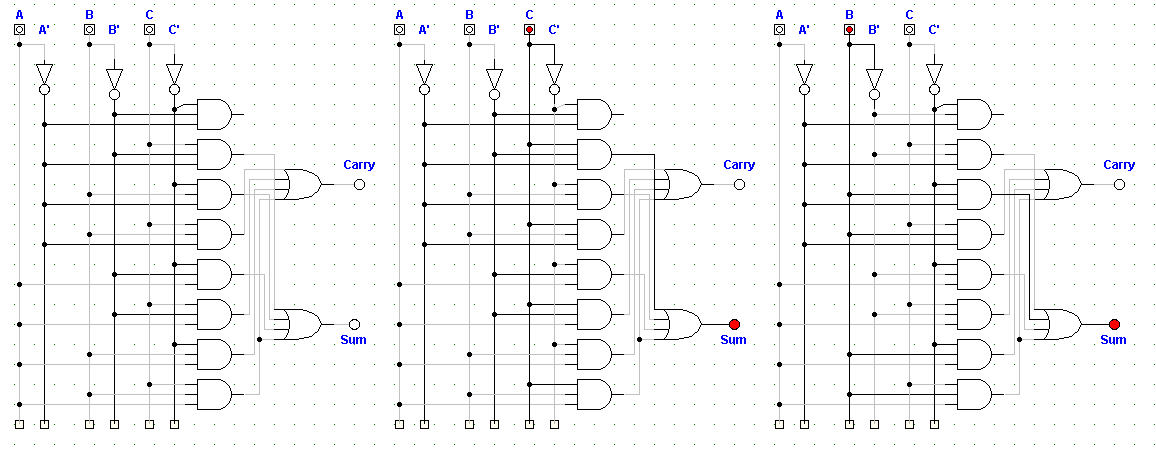
**Circuit Diagram:**

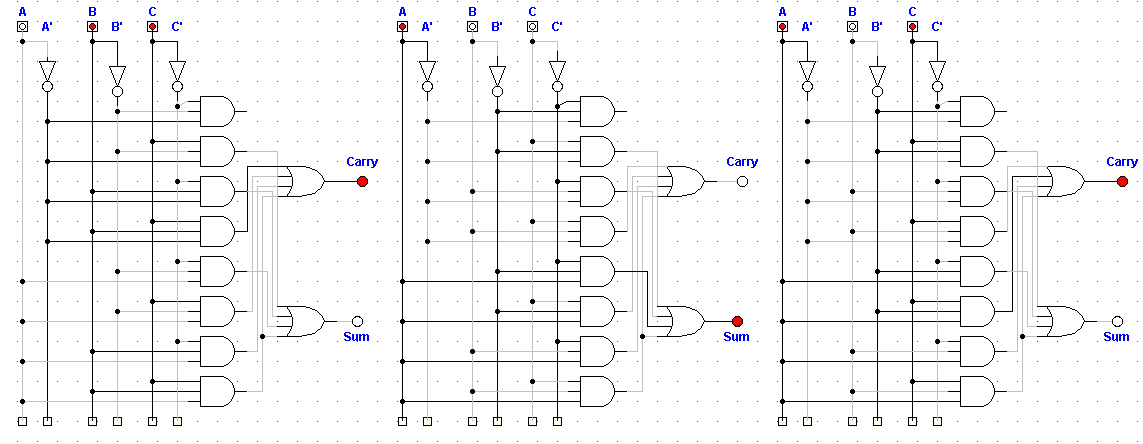
**Fig. Circuit diagram of a full adder using a decoder**

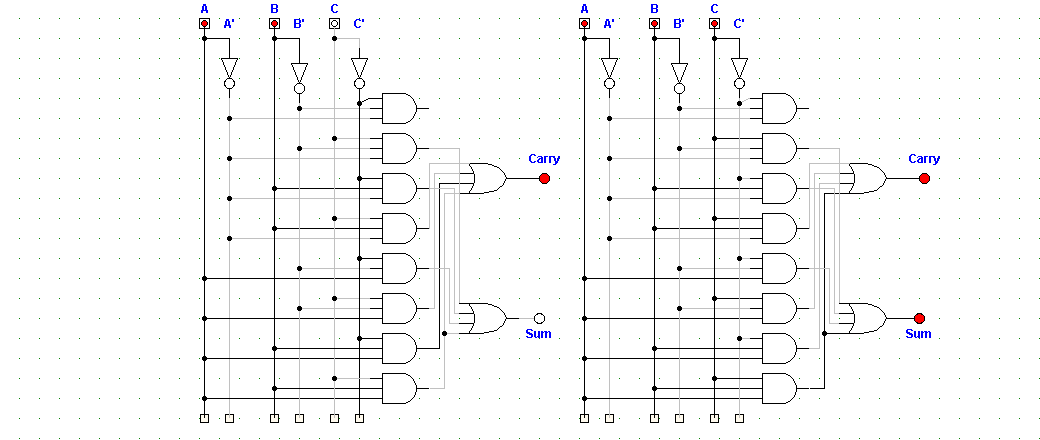
**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Observation:**







**Observation Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Conclusion:**

Thus, the operation of full adder using decoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/3036

http://answers.yahoo.com/question/index?qid=20090215044042AAxpa1T

**OBJECTIVE 1.3**

**To Construct and verify the operation of 2x1 Encoder**

**THEORY:**

An encoder is a digital circuit that essentially performs the inverse function of a decoder. It accepts an active level on one of its inputs representing a digit, such as decimal or octal digit and converts it to a coded output such as BCD or binary. The process of converting input numbers to a coded format is called encoding.

It has 21 inputs and 1 output.

**Boolean Expression:**

A = D1

**Block Diagram:**

**2 x 1 Encoder**

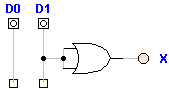
**D0**

**A**

**D1**

**Fig. Block diagram of a 2 x 1 Encoder**

**Circuit Diagram:**

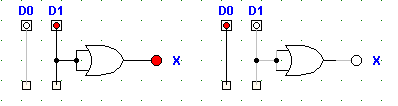
****

**Fig. Circuit diagram of a 2 x 1 Encoder**

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **Input** | | **Output** |
| **D0** | **D1** | **A** |
| 1 | 0 | 0 |
| 0 | 1 | 1 |

**Observation:**

****

**Observation Table:**

|  |  |  |
| --- | --- | --- |
| **Input** | | **Output** |
| **D0** | **D1** | **A** |
| 1 | 0 | 0 |
| 0 | 1 | 1 |

**Conclusion:**

Thus, the operation of 2 x 1 encoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/3036

http://answers.yahoo.com/question/index?qid=20090215044042AAxpa1T

OBJECTIVE 1.4

**To Construct and verify the operation of 4x2 Encoder**

THEORY:

An encoder is a digital circuit that essentially performs the inverse function of a decoder. It accepts an active level on one of its inputs representing a digit, such as decimal or octal digit and converts it to a coded output such as BCD or binary. The process of converting input numbers to a coded format is called encoding.

It has 22 inputs and 2 output.

**Boolean Expression:**

X= D2 + D3

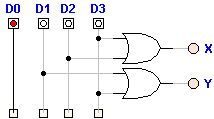
Y= D1 + D3

**Block Diagram:**

**4 X 2 Encoder**

**Fig. Block diagram of a 4 x 2 Encoder**

**Circuit Diagram:**

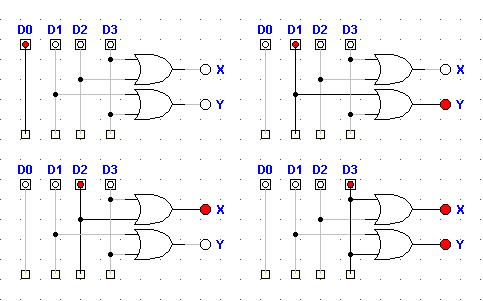
****

**Fig. Circuit diagram of a 4 x 2 Encoder**

**Truth Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input** | | | | **Output** | |
| **D0** | **D1** | **D2** | **D3** | **X** | **Y** |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |

**Observation:**



**Observation Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input** | | | | **Output** | |
| **D0** | **D1** | **D2** | **D3** | **X** | **Y** |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |

**Conclusion:**

Thus, the operation of 4 x 2 encoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/3036

http://answers.yahoo.com/question/index?qid=20090215044042AAxpa1T

**OBJECTIVE 1.5**

**To Construct and verify the operation of 8x3 Encoder**

**THEORY:**

An encoder is a digital circuit that essentially performs the inverse function of a decoder. It accepts an active level on one of its inputs representing a digit, such as decimal or octal digit and converts it to a coded output such as BCD or binary. The process of converting input numbers to a coded format is called encoding.

It has 23 inputs and 3 outputs.

**Boolean Expression:**

X= D4+D5+D6+D7

Y= D2+D3+D6+D7

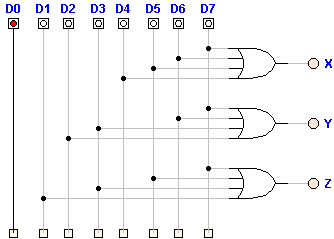
Z= D1+D3+D5+D7

**Block Diagram:**

**8 X 3 Encoder**

**Fig. Block diagram of a 8 x 3 Encoder**

**Circuit Diagram:**

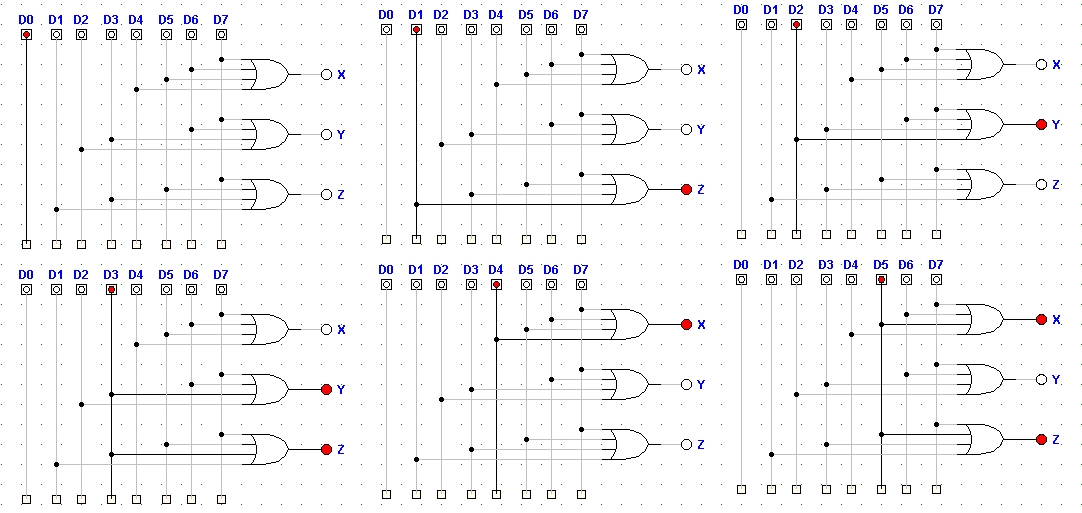
****

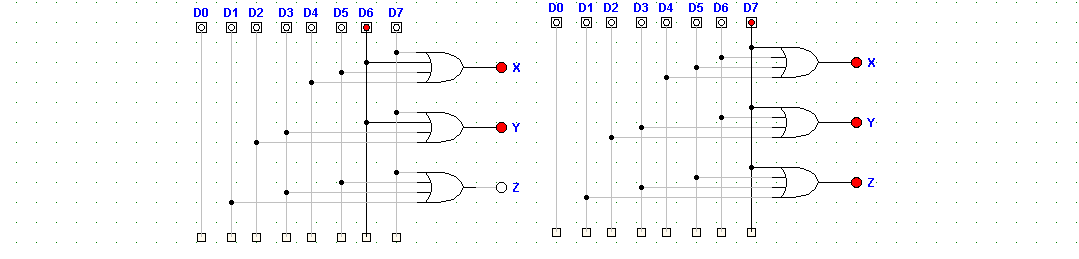
**Fig. Circuit diagram of a 8 x 3 Encoder**

**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | | | | | | | | Output | | |
| D0 | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **X** | **Y** | **Z** |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Observation:**





**Observation Table:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | | | | | | | | **Output** | | |
| **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **X** | **Y** | **Z** |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**Conclusion:**

Thus, the operation of 8 x 3 encoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/3036

http://answers.yahoo.com/question/index?qid=20090215044042AAxpa1T

**OBJECTIVE 1.6**

**To Construct and verify the operation of Decimal to BCD Encoder**

**THEORY:**

An encoder is a digital circuit that essentially performs the inverse function of a decoder. It accepts an active level on one of its inputs representing a digit, such as decimal or octal digit and converts it to a coded output such as BCD or binary. The process of converting input numbers to a coded format is called encoding.

It has 10 inputs and 4 outputs.

**Boolean Expression:**

W= D8+D9

X= D4+D5+D6+D7

Y= D2+D3+D6+D7

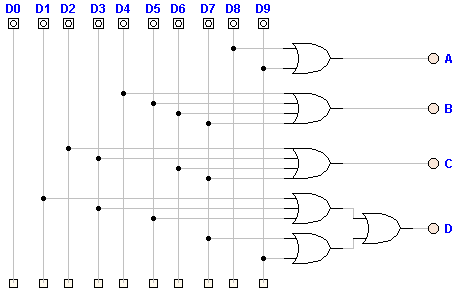
Z= D1+D3+D5+D7+D9

**Block Diagram:**

**Decimal to BCD Encoder**

**Fig. Block diagram of a decimal to BCD Encoder**

**Circuit Diagram:**

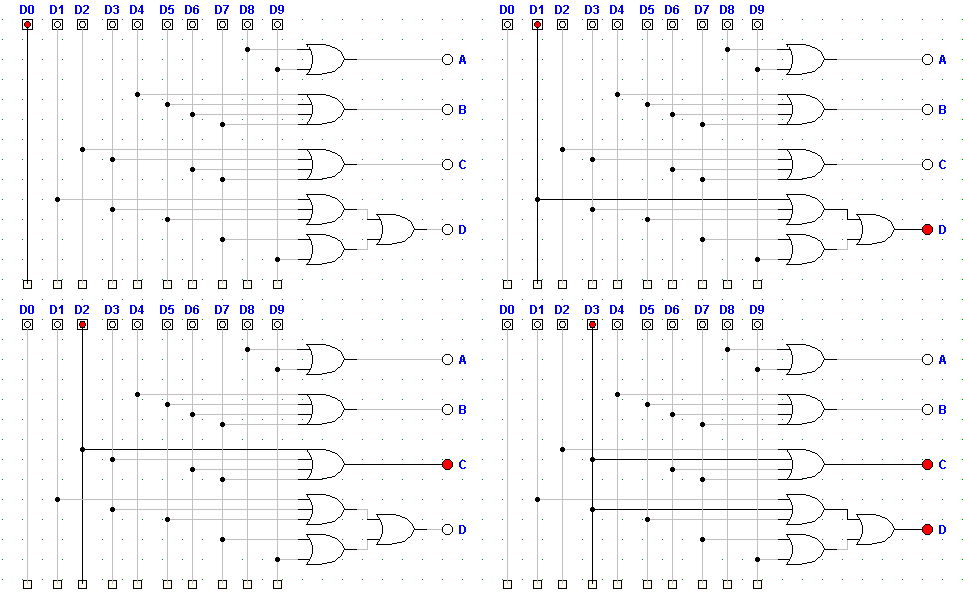
****

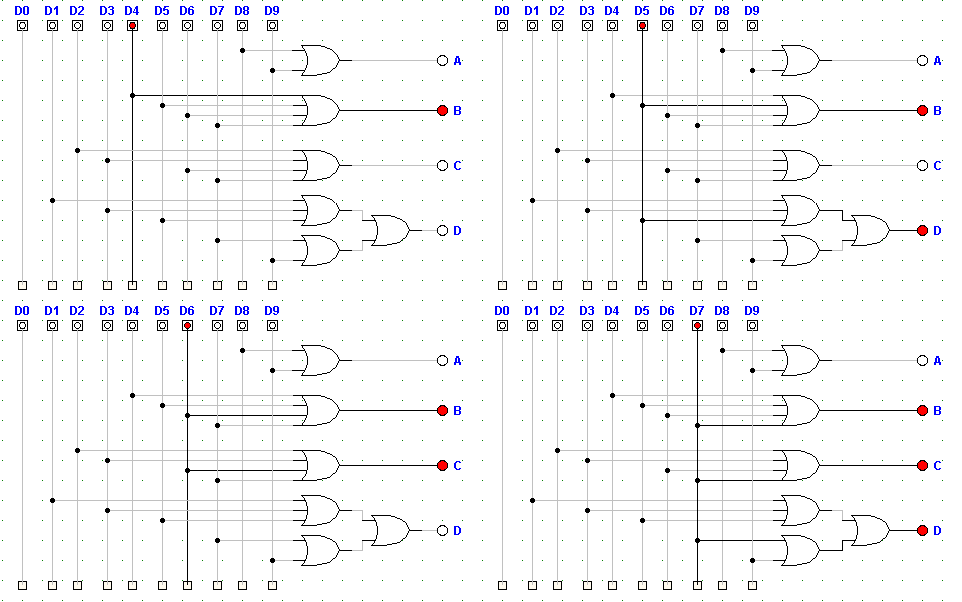
**Fig. Circuit diagram of a Decimal to BCD Encoder**

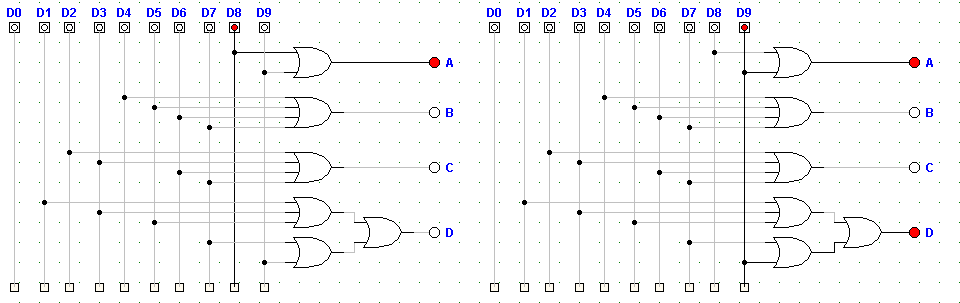
**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | | | | | | | | | | **Output** | | | |
| **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **W** | **X** | **Y** | **Z** |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

**Observation:**







**Observation Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | | | | | | | | | | **Output** | | | |
| **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **W** | **X** | **Y** | **Z** |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

**Conclusion:**

Thus, the operation of Decimal to BCD Encoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/3036

http://answers.yahoo.com/question/index?qid=20090215044042AAxpa1T

**OBJECTIVE 1.7**

**To Construct and verify the operation of 16 x 4 Encoder**

**THEORY:**

An encoder is a digital circuit that essentially performs the inverse function of a decoder. It accepts an active level on one of its inputs representing a digit, such as decimal or octal digit and converts it to a coded output such as BCD or binary. The process of converting input numbers to a coded format is called encoding.

It has 24 inputs and 4 outputs.

**Boolean Expression:**

A = D8+D9+D10+D11+D12+D13+D14+D15

B= D4+D5+D6+D7+ D12+D13+D14+D15

C= D2+D3+D6+D7+D10+D11+D14+D15

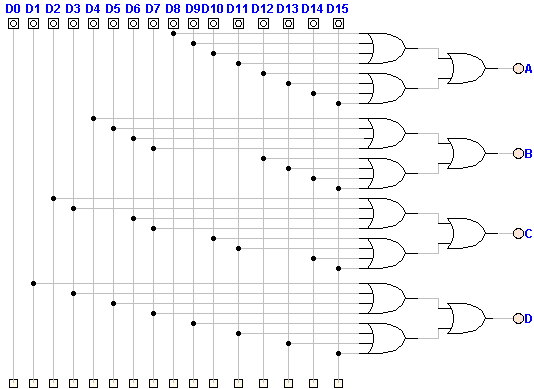
D= D1+D3+D5+D7+D9+D11+D13+D15

**Block Diagram:**

**16 X 4 Encoder**

**Fig. Block diagram of a 16 x 4 Encoder**

**Circuit Diagram:**

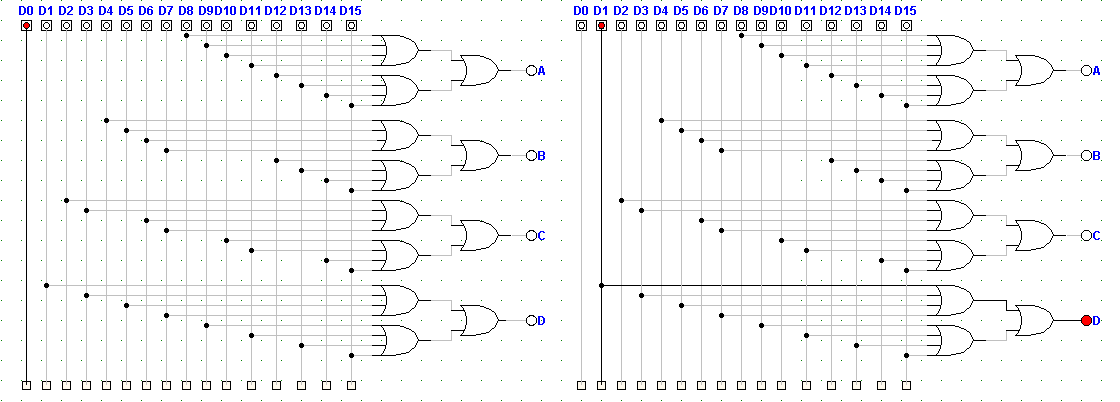
****

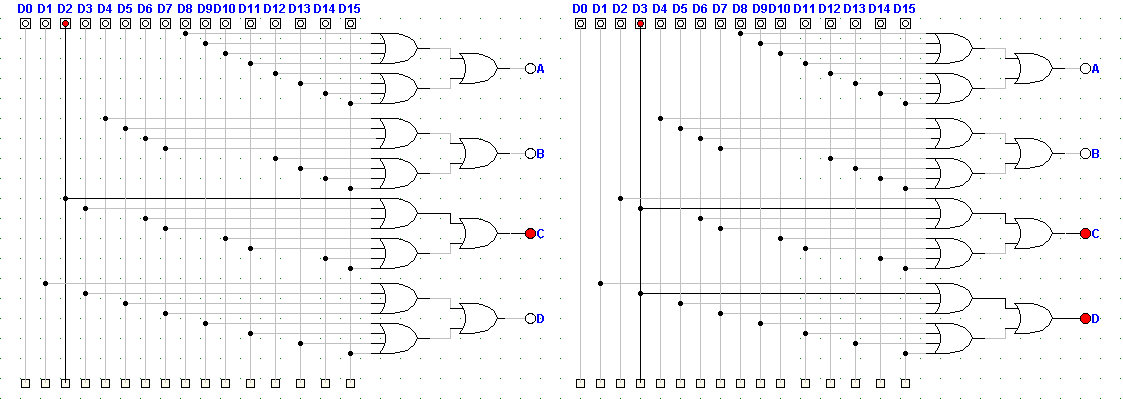
**Fig. Circuit diagram of a 16 x 4 Encoder**

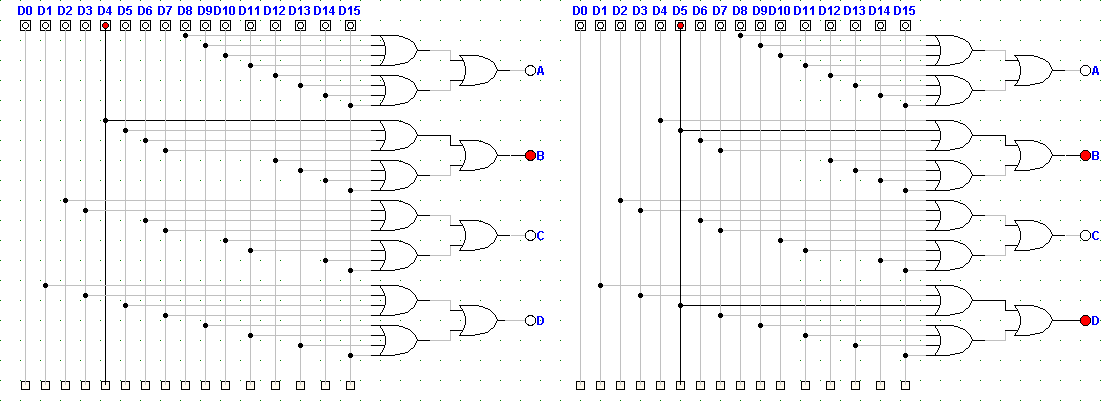
**Truth Table:**

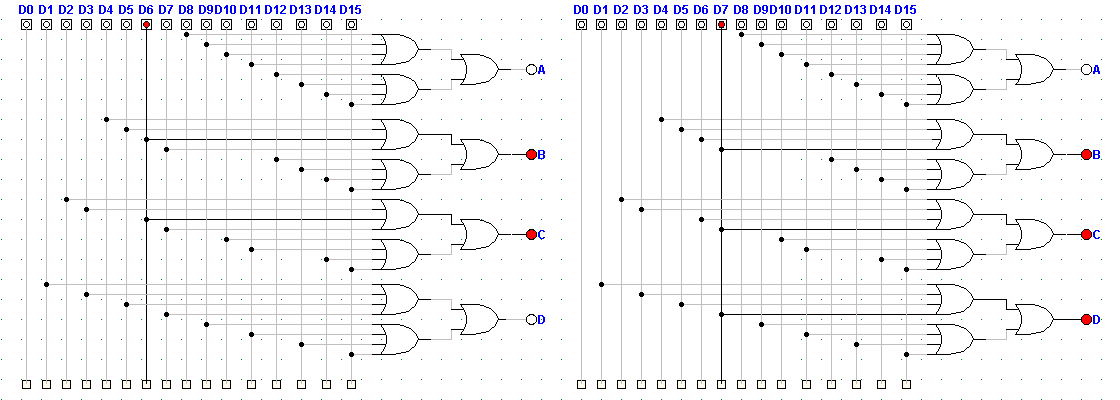
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | | | | | | | | | | | | | | | | **Output** | | | |
| 1 | 1 | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** | **D11** | **D12** | **D13** | **D14** | **D15** | **W** | **X** | **Y** | **Z** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

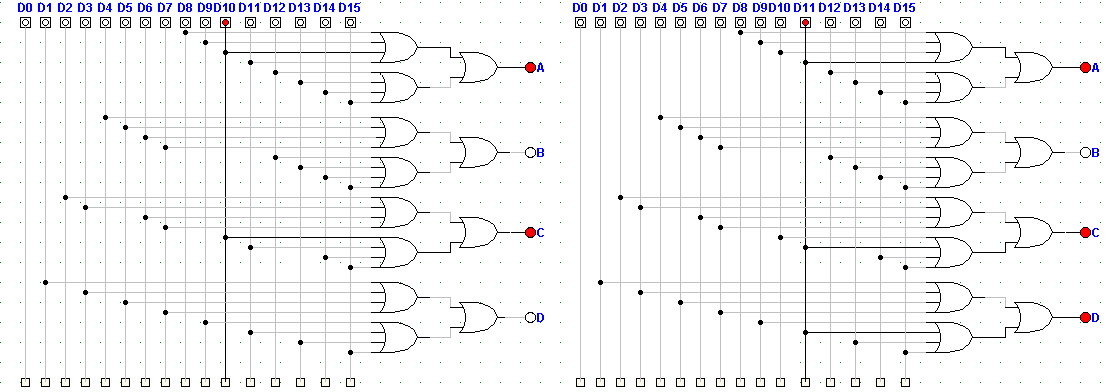
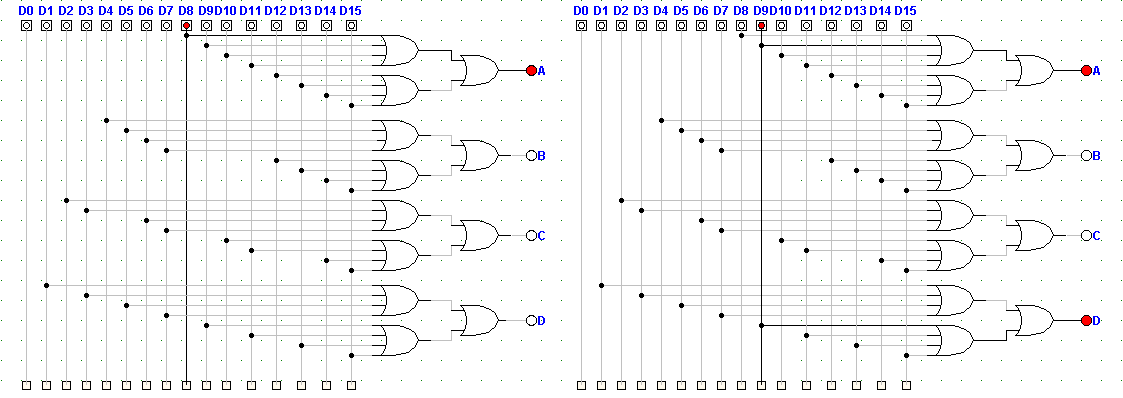
**Observation:**

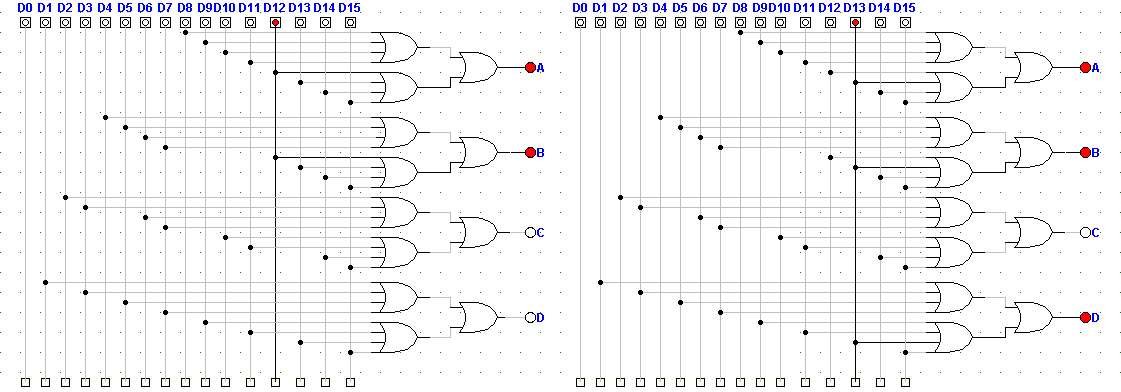


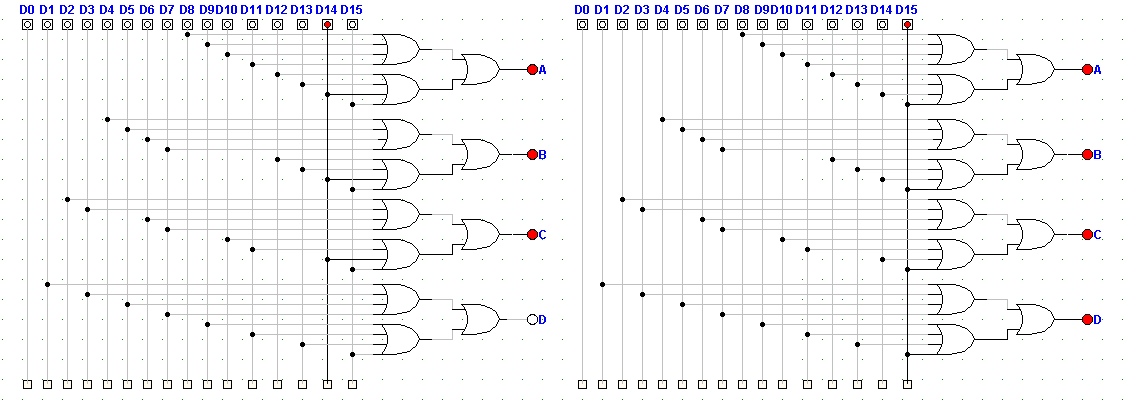












**Observation Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | | | | | | | | | | | | | | | | **Output** | | | |
| 1 | 1 | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** | **D11** | **D12** | **D13** | **D14** | **D15** | **W** | **X** | **Y** | **Z** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**Conclusion:**

Thus, the operation of 16 x 4 encoder was constructed and verified.

**Reference:**

http://www.ustudy.in/node/30